REMARKS

I. Introduction

In response to the Office Action dated August 23, 2004, Applicants have canceled claims 23-24, without prejudice or disclaimer. Applicants have also amended claim 6 so as to address the pending rejection under 35 U.S.C. § 112, second paragraph. Support for this amendment can be found, for example, at page 18, line 19 to page 20, line 10. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 6, 8-11 and 21-24 Under 35 U.S.C. § 112, Second Paragraph

Claims 6, 8-11 and 21-24 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner asserts that the claim limitation "transferring said processing specification information through said at least one internal data bus in a batch" is indefinite, because there is only one specification information in the first area to be transferred and only one resultant data to be written.

However, contrary to the conclusion set forth in the Office Action, as readily shown in Fig. 6 of Applicants' drawings, a first memory cell group 101 is connected with a first word line group 100 in the memory array A, where a plurality of memory cells belonging to the first memory cell group 101 store data processing specification information for the data processor 30'. Specifically, the data processing specification information in each memory cell of the first memory cell group 101 is loaded into the data processor 30' from the memory array A through the hyper-wide but data buses 60. As such, there is NOT only "one" specification information in the first area for transferring, and

"one" resultant data to be written, as concluded by the Examiner. Rather, the data processing specification information comprising connection information of the switching matrix S columns 50 and program information of the program logics PL stored in each memory cell of the first memory cell group 101 are transferred, and the resultant processed data are then stored in the memory cells of the third memory cell group 105 of the memory array B (see, e.g, page 19, line 23 to page 20, line 7 of the specification).

However, in an effort to advance the prosecution expeditiously, the foregoing claim language has been deleted, and replaced with "transferring said processing specification information through said at least one internal data bus in parallel to said reconfigurable logic circuit, said processing specification information determining logical connections of said reconfigurable logic circuit." It is respectfully submitted that the foregoing amendment to claim 6 overcomes the pending rejection under 35 U.S.C. § 112, second paragraph.

III. The Rejection Of Claims 6, 8, 23 and 24 Under 35 U.S.C. § 103

Claims 6, 8, 23 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 5,968,160 to Saito in view of USP No. 5,535,410 to Watanabe. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 6 recites in-part a data processing method comprising the steps of 1) writing a processing specification information in a first area corresponding to a first word line within a semiconductor device comprising at least one memory array and a reconfigurable logic circuit coupled to the at least one memory array through at least one internal data bus, 2) transferring the processing specification information through the at least one internal data bus in parallel to the reconfigurable logic circuit, the processing specification information determining logical

connections of the reconfigurable logic circuit, 3) transferring the data through the at least one internal data bus in parallel to the reconfigurable logic circuit, and 4) processing the data by the reconfigurable logic circuit according to the processing specification information and writing resultant processed data through the at least one internal data bus in parallel in a third area corresponding to a third word line within the semiconductor device.

In accordance with one embodiment of the present invention, the data for determining the logical connection of the reconfigurable logic circuit is transmitted from the memory array to the reconfigurable logic circuit via the internal bus. Specifically, using the same data bus utilized for the data for determining the logical connection of the reconfigurable logic circuit, the data to be processed is transmitted to the reconfigurable logic circuit. Based on this configuration, the internal data bus can be effectively utilized with a wide data bus width. Also, the data for determining the processing specification information is transmitted to the reconfigurable logic circuit using the same data bus as utilized for transmitting the data to be processed thereto. The foregoing method allows for performing a complicated processing of data while flexibly restructuring the logic in the reconfigurable logic circuit.

Turning to the cited prior art, the Examiner admits that Saito is silent with regard to providing a data processor comprising reconfigurable logic, but alleges that Watanabe discloses, at col. 2, lines 3-11, a parallel processor for performing parallel processing by switching between the single instruction multiple data stream (SIMD) and multiple instruction multiple data stream (MIMD) operations (see, page 6, item 7 of Office Action).

However, contrary to the conclusion set forth by the Examiner, nowhere does Saito or Watanabe, taken alone or in combination, discuss or even recognize any reconfigurable logic circuit in the manner asserted in the pending Office Action. Indeed, at the cited portion, Watanabe

discloses providing a parallel processor utilizing a memory cell array for dealing with applications using a mixture of SIMD and MIMD operation modes, such that the processor loses little time in switching between the two modes of operations so as to control the configured processing elements efficiently in keeping with the degree of parallelism. More specifically, Watanabe doscloses that the processing elements PE1-PEn are controlled in one of SIMD and MIMD operation modes. These operation modes are switched over by an external operation mode switching signal ø S/M controlling the group switches SW-OP. For example, when the operation mode switching signal ø S/M is logic High, the SIMD operation mode is selected, and when the operation mode switching signal ø S/M is logic Low, the MIMD operation mode is selected. As such, the switching between SIMD and MIMD operation modes is controlled by the external switching signal ø S/M, which is independent of the data in the memory array (see, Fig. 1, and col. 3, line 66 to col. 4, line 1).

Thus, at a minimum, Saito and Watanabe, taken alone or in combination, do not disclose or suggest any reconfigurable logic circuit coupled to the at least one memory array through at least one internal data bus. In doing so, Saito and Watanabe, taken alone or in combination, fails to disclose or suggest a data processing method comprising the steps of 1) writing a processing specification information in a first area corresponding to a first word line within a semiconductor device comprising at least one memory array and a reconfigurable logic circuit coupled to the at least one memory array through at least one internal data bus, 2) transferring the processing specification information through the at least one internal data bus in parallel to the reconfigurable logic circuit, the processing specification information determining logical connections of the reconfigurable logic circuit, 3) transferring the data through the at least one internal data bus in parallel to the reconfigurable logic circuit, and 4) processing the data by the reconfigurable logic circuit according to the processing specification information and writing resultant processed data

through the at least one internal data bus in parallel in a third area corresponding to a third word line within the semiconductor device, as recited by claim 6.

As each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and Saito and Watanabe, taken alone or in combination, fail to do so, it is respectfully submitted that claim 6 is patentable over the prior art.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claim 6 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

For all of the foregoing reasons, it is submitted that claims 8-11 and 21-22 are patentable over the cited prior art. Accordingly, it is respectfully submitted that the rejections of claims 6, 8-11 and 21-22 under 35 U.S.C. § 103 have been overcome.

V. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: November 22, 2004